Listing of the Claims

This listing of claims will replace all prior versions and listings of claims in the application. Added text is indicated by underlining, deleted text is indicated by ~~strikethrough~~. Changes are identified by a change bar in the margin.

1. (currently amended) A method of producing a cyclic combinational circuit, the method comprising:

determining cyclic parameters; and

synthesizing a the cyclic combinational circuit in accordance with the determined cyclic parameters.

2. (currently amended) ~~A~~ The method as defined in Claim 1, wherein the determining cyclic parameters further comprises:

defining at least one input variable;

defining at least one output variable; and

defining a relationship between the at least one input and the at least one output variable whereby the relationship includes a cycle.

3. (currently amended) ~~A~~ The method as defined in Claim 2, further including at least one internal variable.

4. (currently amended) ~~A~~ The method as defined in Claim 2, wherein the relationship includes structured dependency between an input variable and an output variable.

5. (currently amended) ~~A~~ The method as defined in Claim 1, wherein the determining cyclic parameters further comprises:

defining at least one input variable;

defining at least one internal variable; and

defining a relationship between the at least one input and the at least one internal variable whereby the relationship includes a cycle.

6. (currently amended) ~~A~~ The method as defined in Claim 5, wherein the at least one internal variable is an output variable.

7. (currently amended) ~~A~~ The method as defined in Claim 5, wherein the relationship includes structured dependency between an input variable and an internal variable.

8. (currently amended) ~~A~~ The method as defined in Claim 1, wherein the determined cyclic parameters are used in a logic synthesis process.

9. (currently amended) ~~A~~ The method as defined in Claim 8, wherein the determined cyclic parameters are used in a structuring operation of the logic synthesis process.

10. (currently amended) ~~A~~ The method as defined in Claim 9, wherein the structuring operation includes a substitution phase of the logic synthesis process.

11. (currently amended) ~~A~~ The method as defined in Claim 1, wherein the method of producing a cyclic combinational circuit is optimized.

12. (currently amended) ~~A~~ The method as defined in Claim 11, wherein the cyclic combinational circuit is optimized with regard to cost.

13. (currently amended) ~~A~~ The method as defined in Claim 12, wherein the cost is measured as an area.

14. (currently amended) ~~A~~ The method as defined in Claim 13, wherein the area is determined by a literal count.

15. (currently amended) ~~A~~ The method as defined in Claim 13, wherein the area is determined by a gate count.

16. (currently amended) ~~A~~ The method as defined in Claim 11, wherein the cyclic combinational circuit is optimized with regard to performance.

17. (currently amended) ~~A~~ The method as defined in Claim 16, wherein the performance is measured as a delay of the combinational circuit.

18. (currently amended) A method of producing a cyclic combinational circuit, the method comprising:

determining cyclic parameters; and

synthesizing the cyclic combinational circuit in accordance with the determined cyclic parameters;

wherein the method of producing a cyclic combinational circuit is optimized, and

~~A method as defined in Claim 11,~~ wherein the cyclic combinational circuit is optimized with regard to fault tolerance.

19. (currently amended) ~~A~~ The method as defined in Claim 11, wherein the cyclic combinational circuit is optimized with regard to power consumption.

20. (currently amended) ~~A~~ The method as defined in Claim 11, wherein the cyclic combinational circuit is optimized with regard to testability.

21. (currently amended) A method of producing a cyclic combinational circuit, the method comprising:

determining cyclic parameters; and

synthesizing the cyclic combinational circuit in accordance with the determined cyclic parameters; and

~~A method as defined in Claim 1,~~ wherein the synthesizing comprises:

creating a network with no cycles;

introducing a cycle into the network;

determining if the network is combinational; and

repeating introduction of cycles into the network until a desired cyclic combinational circuit is implemented.

22. (currently amended) ~~A~~ The method as defined in Claim 21, wherein the cyclic combinational circuit is optimized.

23. (currently amended) ~~A~~ The method as defined in Claim 22, wherein the cyclic combinational circuit is optimized with regard to cost.

24. (currently amended) ~~A~~ The method as defined in Claim 23, wherein the cost is measured as an area.

25. (currently amended) ~~A~~ The method as defined in Claim 24, wherein the area is determined by a literal count.

26. (currently amended) ~~A~~ The method as defined in Claim 24, wherein the area is determined by a gate count.

27. (currently amended) ~~A~~ The method as defined in Claim 22, wherein the cyclic combinational circuit is optimized with regard to performance.

28. (currently amended) ~~A~~ The method as defined in Claim 27, wherein the performance is measured as a delay of the cyclic combinational circuit.

29. (currently amended) ~~A~~ The method as defined in Claim 22, wherein the cyclic combinational circuit is optimized with regard to fault tolerance.

30. (currently amended) ~~A~~ The method as defined in Claim 22, wherein the cyclic combinational circuit is optimized with regard to power consumption.

31. (currently amended) ~~A~~ The method as defined in Claim 22, wherein the cyclic combinational circuit is optimized with regard to testability.

32. (currently amended) The method as defined in Claim 21, wherein the introducing, the determining and the repeating are ~~is~~ performed in a structuring operation of logic synthesis.

33. (currently amended) ~~A~~ The method as defined in claim 32, wherein the structuring operation includes a substitution phase of logic synthesis.

34. (currently amended) A method of producing a cyclic combinational circuit, the method comprising:

determining cyclic parameters; and

synthesizing the cyclic combinational circuit in accordance with the determined cyclic parameters;

~~A method as defined in Claim 1,~~ wherein the synthesizing comprises:

creating a densely interconnected network;

excluding edges from the densely interconnected network;

determining if the densely interconnected network is combinational; and

repeating the excluding edges ~~the~~ from the densely interconnected network until a desired cyclic combinational circuit is implemented.

35. (currently amended) ~~A~~ The method as defined in Claim 34 wherein the desired cyclic combinational circuit is optimized.

36. (currently amended) ~~A~~ The method as defined in Claim 35, wherein the desired cyclic combinational circuit is optimized with regard to cost.

37. (currently amended) ~~A~~ The method as defined in Claim 36, wherein the cost is measured as an area.

38. (currently amended) ~~A~~ The method as defined in Claim 37, wherein the area is determined by a literal count.

39. (currently amended) ~~A~~ The method as defined in Claim 37, wherein the area is determined by a gate count.

40. (currently amended) ~~A~~ The method as defined in Claim 35, wherein the desired cyclic combinational circuit is optimized with regard to performance.

41. (currently amended) ~~A~~ The method as defined in Claim 40, wherein the performance is measured as a delay of the combinational circuit.

42. (currently amended) ~~A~~ The method as defined in Claim 35, wherein the desired cyclic combinational circuit is optimized with regard to fault tolerance.

43. (currently amended) ~~A~~ The method as defined in Claim 35, wherein the desired cyclic combinational circuit is optimized with regard to power consumption.

44. (currently amended) ~~A~~ The method as defined in Claim 35, wherein the desired cyclic combinational circuit is optimized with regard to testability.

45. (currently amended) The method as defined in Claim 34, wherein the introducing, the determining and the repeating is performed in a structuring operation of logic synthesis.

46. (currently amended) ~~A~~ The method as defined in claim 45, wherein the structuring operation includes a substitution phase of logic synthesis.

47. (currently amended) A method of logic synthesis, the method comprising:
determining cyclic parameters; and
using the cyclic parameters during synthesis of a cyclic combinational circuit.

48. (currently amended) ~~A~~ The method as defined in Claim 47, wherein the determined cyclic parameters are used in a structuring operation of logic synthesis.

49. (currently amended) ~~A~~ The method as defined in Claim 48, wherein the structuring operation includes a substitution phase of the logic synthesis.

50. (currently amended) A logic synthesizer comprising:
a logic for determining a set of cyclic parameters; and

a processor configured to synthesize a cyclic combinational circuit in accordance with the determined set of cyclic parameters.

51. (currently amended) ~~A~~ The logic synthesizer as defined in Claim 50, wherein the determined set of cyclic parameters further comprises:

at least one input variable;

at least one output variable; and

a relationship between the at least one input variable and at least one output variable whereby the relationship includes a cycle.

52. (currently amended) ~~A~~ The logic synthesizer as defined in Claim 51, further including at least one internal variable.

53. (currently amended) ~~A~~ The logic synthesizer as defined in Claim 51, wherein the relationship includes structured dependency between an input variable and an output variable.

54. (currently amended) ~~A~~ The logic synthesizer as defined in Claim 50, wherein the determined set of cyclic parameters further comprises:

at least one input variable;

at least one internal variable; and

a relationship between the at least one input variable and the at least one internal variable whereby the relationship includes a cycle.

55. (currently amended) ~~A~~ The logic synthesizer as defined in Claim 54, wherein the at least one internal variable is an output variable.

56. (currently amended) ~~A~~ The logic synthesizer as defined in Claim 54, wherein the relationship includes structured dependency between an input variable and an internal variable.

57. (currently amended) ~~A~~ The logic method as defined in Claim 50, wherein the determined set of cyclic parameters are used in a logic synthesis process.

58. (currently amended) ~~A~~ The logic synthesizer as defined in Claim 57, wherein the determined set of cyclic parameters are used in a structuring operation of the logic synthesis process.

59. (currently amended) ~~A~~ The logic synthesizer as defined in Claim 58, wherein the structuring operation includes a substitution phase of the logic synthesis process.

60. (currently amended) ~~A~~ The logic synthesizer as defined in Claim 50, wherein the synthesized cycliccombinational circuit is optimized.

61. (currently amended) ~~A~~ The logic synthesizer as defined in Claim 60, wherein the cyclic combinational circuit is optimized with regard to cost.

62. (currently amended) ~~A~~ The logic synthesizer as defined in Claim 61, wherein the cost is measured as an area.

63. (currently amended) ~~A~~ The logic synthesizer as defined in Claim 62, wherein the area is determined by a literal count.

64. (currently amended) ~~A~~ The logic synthesizer as defined in Claim 62, wherein the area is determined by a gate count.

65. (currently amended) ~~A~~ The logic synthesizer as defined in Claim 60, wherein the cyclic combinational circuit is optimized with regard to performance.

66. (currently amended) ~~A~~ The logic synthesizer as defined in Claim 65, wherein the performance is measured as a delay of the cyclic combinational circuit.

67. (currently amended) A logic synthesizer comprising:

a logic for determining a set of cyclic parameters; and

a processor configured to synthesize a cyclic combinational circuit in accordance with the determined set of cyclic parameters;

wherein the synthesized cyclic combinational circuit is optimized; and

~~A synthesizer as defined in Claim 60,~~ wherein the cyclic combinational circuit is optimized with regard to fault tolerance.

68. (currently amended) ~~A~~ The logic synthesizer as defined in Claim 60, wherein the cyclic combinational circuit is optimized with regard to power consumption.

69. (currently amended) ~~A~~ The logic synthesizer as defined in Claim 60, wherein the cyclic combinational circuit is optimized with regard to testability.

70. (currently amended) A logic synthesizer comprising:

a logic for determining a set of cyclic parameters; and

a processor configured to synthesize a cyclic combinational circuit in accordance with the determined set of cyclic parameters;

~~A synthesizer as defined in Claim 50,~~ wherein the processor creates a network with no cycles, and then introduces cycles into the network and determines if the network is combinational, and then it repeats introducing cycles into the network until a desired cyclic

combinational circuit~~,~~ is implemented.

71. (currently amended) A logic synthesizer comprising:

a logic for determining a set of cyclic parameters; and

a processor configured to synthesize a cyclic combinational circuit in accordance with the determined set of cyclic parameters;

~~A synthesizer as defined in Claim 50,~~ wherein the processor creates a densely interconnected network, and then excludes edges from the densely interconnected network and determines if the densely interconnected network is combinational, and then repeats excluding edges from the densely interconnected network until a desired cyclic combinational circuit is implemented.